Parallelization techniques of HPCG and evaluation on Arm based platforms

Dani Ruiz
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HPCG benchmark is a complementary benchmark to HPL and represents current HPC workloads

- But no Arm based platform on the TOP500 yet!
- Need of an optimized version
SIMD parallelization

- Compilers aren’t equal for different architectures

- Write NEON code manually
- Wait for smarter compiler
- Use different SIMD extension

Same compiler
NEON instr << AVX512 instr
Memory access evaluation

- Cache hit ratio degraded when using multi-coloring approaches

- What if we could choose what to have on cache?
  - “Cache programming”

- What if we could load non-contiguous memory locations to a SIMD register?
  - Gather-load instruction

~13% L1D miss ratio
~35% L2D miss ratio
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montblanc-project.eu  @MontBlanc_EU  daniel.ruiz@bsc.es